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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
ONO et al.	**Art Unit 2816**
Patent Number: 6,847,252 B1	
Issued : January 25, 2005	
Application Number: 10/671,477	**Examiner Englund, Terry Lee**
Filed: September 29, 2003	
For: WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD (AS AMENDED)	
Attorney Docket No. NITT.0156	

Certificate
FEB 2 5 2005
of Correction

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

LETTER

Sir:

The below-identified communications are submitted in the above-captioned application or proceeding:

(1) Copy of Request for Certificate of Correction
(2) Certificate of Correction Form 1050
(3) Copy of Response to Office Action dated September 29, 2004
(4) Copy of Issue Fee Payment Transmittal dated November 12, 2004

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17 or credit any overpayment to **Deposit Account Number 08-1480**. A duplicate copy of this sheet is attached.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200
FEBRUARY 22, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
ONO et al.	)	**Art Unit 2816**
	)	
Patent Number: 6,847,252 B1	)	
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Issued : January 25, 2005	)	
	)	
Application Number: 10/671,477	)	**Examiner**
	)	**Englund, Terry Lee**
Filed: September 29, 2003	)	
	)	
For: WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD (AS AMENDED)	)	
	)	
Attorney Docket No. NITT.0156	)	

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

The Commissioner is hereby respectfully requested to grant a Certificate of Correction in accordance with the attached Certificate of Correction. The title of the invention is incorrect and should read as "**WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD**". Attached is a copy of the Form PTO-1050, setting forth the requested change.

The title of the invention was amended on September 29, 2004 in a response to the Office Action to "**WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD**" as suggested by the Examiner in an Office Action dated June 29, 2004. However, in the Notice of Allowance dated October 20, 2004, the title was not amended. Nevertheless, the title was correctly reflected on the Issue Fee Transmittal filed on November 12, 2004.

The Applicants hereby attach (1) a copy of the Form PTO-1050, 2) a copy of the Response to the Office Action dated September 29, 2004 (3) a copy of the Issue Fee Payment Transmittal dated November 12, 2004.

Since the correction being requested appears to have resulted from an error on the part of the U.S. Patent and Trademark Office, no fee is required. However, the Commissioner is hereby authorized to charge payment of any fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17 or credit any overpayment to **Deposit Account Number 08-1480**.

Respectfully submitted,

Stanley P. Fisher
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FEBRUARY 22, 2005

PTO/SB/44 (04-04)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,252 B1

DATED : January 25, 2005

INVENTOR(S) : Ono et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (54):

Please delete "SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE" and

insert --- **WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD** ---

MAILING ADDRESS OF SENDER:

PATENT NO. 6,847,252 B1
No. of additional copies ___

Stanley P. Fisher, Esq.
Reed Smith LLP
Suite 1400
3110 Fairview Park Drive
Falls Church, VA 22042

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
ONO et al.	)	**Art Unit 2816**
	)	
Application Number: 10/671,477	)	**Examiner**
	)	**Englund, Terry Lee**
Filed: September 29, 2003	)	
	)	
For: WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD (AS AMENDED)	)	
	)	
Attorney Docket No. NITT.0156	)	

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

COVER LETTER

Sir:

[x] The fee for submission of claims is calculated as shown below:

FOR	TOTAL WITH NEW CLAIMS ADDED	TOTAL CURRENTLY ON FILE	CLAIMS PAID	RATE	CALCULATION
Total Claims	14	14	(Over 20)	x $18	0
Independent Claims	2	2	(Over 3)	x $84	0
MULTIPLE DEPENDENT CLAIM(S)				+ $280	0
REDUCTION FOR FILING BY SMALL ENTITY (note 37 C.F.R. §§ 1.9, 1.27, 1.28). IF APPLICABLE, VERIFIED STATEMENT MUST BE ATTACHED				x ½	
			TOTAL		0.00

In addition, the below-identified communications are submitted in the above-captioned application or proceeding:

[x] Response to Office Action (with Claim Amendments)
[ ] Preliminary Amendment
[ ] Substitute Specification
[ ] Other _____

[x] Terminal Disclaimer
[ ] Information Disclosure Statement
[x] Letter to Draftsperson
[x] 2 sheets of drawings
[ ] Petition under _____

[ ] Please charge my **Deposit Account Number** _____ in the amount of _____ to cover the fees for _ _____. A duplicate copy of this paper is enclosed.

[x] A check in the amount of **$110.00** to cover the Terminal Disclaimer fee is enclosed.

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17, or credit any overpayment to **Deposit Account Number 08-1480.**

Respectfully submitted,

_____

Stanley P. Fisher
Registration Number 24,344

_____

Juan Carlos A. Marquez
Registration No. 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200
September 29, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
ONO et al.	)	**Art Unit 2816**
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Application Number: 10/671,477	)	**Examiner**
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	)	
For: WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD (AS AMENDED)	)	
	)	
Attorney Docket No. NITT.0156	)	

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

RESPONSE AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

This is in response to the Office Action dated June 29, 2004, the period for response to which expires on September 29, 2004. Please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the Title the Invention currently on file with the following title:

"Well Bias Voltage Control Circuit And Method"

Please amend the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file as follows:

This application is a Continuation of nonprovisional application serial number 10/284,207 filed October 31, 2002, which was issued into U.S. Patent No. 6,653,890 on Nov. 25, 2003. Priority is claimed based on U.S. application No. 10/284,207 filed October 31, 2002, which claims the priority of Japanese application 2001-336208 filed on November 1, 2001.

Please amend the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file as follows:

In the second embodiment, in a manner similar to the first embodiment, the delay of the CMOS LSI can be compensated and the threshold voltage difference between the PMOS transistor and the NMOS transistor can be eliminated. In addition, by feeding back the signal vbap to the PN Vt balance compensation circuit 123, even if the threshold voltage difference occurs between the PMOS transistor and the NMOS transistor at the time of changing the signals vbap and vban in order to compensate delay, the difference can be compensated.

IN THE ABSTRACT

Please replace the Abstract of the Disclosure currently on file with the attached substitute Abstract.

Abstract

A semiconductor integrated circuit device having a mechanism of compensating not only circuit operational speed but also variations in leakage current, which includes: a main circuit constructed with CMOS device, a delay monitor for simulating a critical path of the main circuit constructed by a CMOS and monitoring a delay of the path, a PN Vt balance compensation circuit for detecting a threshold voltage difference between a PMOS transistor and an NMOS transistor, and a well bias generating circuit for receiving outputs of the delay monitor and the PN Vt balance compensation circuit and applying a well bias to the delay monitor and the main circuit so as to compensate the operation speed of the delay monitor to a desired speed and reduce a threshold voltage difference between the PMOS and NMOS transistors.

IN THE CLAIMS:

Please amend claims 1-6 and 8-14 as follows:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a first circuit comprising a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type,

a delay monitor circuit comprising a third MOS transistor of the first conductivity type and a fourth MOS transistor of the second conductivity type, and outputting a delay signal,

a first comparator comparing the delay signal with a clock signal and outputting a first control signal and a second control signal,

a well bias voltage generator outputting a first well bias voltage to the first MOS transistor and the third MOS transistor and outputting a second well bias voltage to the second MOS transistor and the fourth MOS transistor, and

a compensation circuit comprising a fifth MOS transistor of the first conductivity type and a sixth MOS transistor of the second conductivity type, and outputting a difference signal, the difference signal based on the difference between a threshold voltage of the fifth MOS transistor and a threshold voltage of the sixth MOS transistor,

wherein the well bias voltage generator outputs the first well bias voltage controlled by the first control signal and outputs the second well bias voltage controlled by the second control signal adjusted by the difference signal.

2. (Currently Amended) A semiconductor integrated circuit device according to claim 1,

wherein the compensation circuit further comprises,

a first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor and outputting a first logical threshold voltage,

a reference voltage generator outputting a first reference voltage and a second reference voltage lower than the first reference voltage,

a second comparator comparing the first logical threshold voltage with the first and second reference voltages, and outputting a first signal and a second signal, and

a difference detector detecting the difference between the first signal and the second signal, and outputting the difference signal.

3. (Currently Amended) A semiconductor integrated circuit device according to claim 2, wherein the second comparator outputs the first signal when the first logical threshold voltage is higher than the first reference voltage, and outputs the second signal when the first logical threshold voltage is lower than the second reference voltage.

4. (Currently Amended) A semiconductor integrated circuit device according to claim 1, wherein the compensation circuit further comprises,

a first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor and outputting a first logical threshold voltage,

a second comparator comprising a second CMOS inverter having a second logical threshold voltage, and a third CMOS inverter having a third logical threshold voltage lower than the second logical threshold voltage, comparing the first logical threshold voltage with the second and third threshold voltages and outputting a first signal and a second signal, and

a difference detector detecting the difference between the first signal and the second signal, and outputting the difference signal.

5. (Currently Amended) A semiconductor integrated circuit device according to claim 4, wherein the second comparator outputs the first signal when the first logical threshold voltage is higher than the second logical threshold voltage, and outputs the second signal when the first logical threshold voltage is lower than the third logical threshold voltage.

6. (Currently Amended) A semiconductor integrated circuit device according to claim 1, wherein the well bias voltage generator changes the second control signal in comparison to the first control signal based on the difference signal by using a table lookup method.

7. (Original) A semiconductor integrated circuit device according to claim 1, wherein the first circuit further comprises a critical path comprising the first MOS transistor and the second MOS transistor, and having a delay time,

wherein the delay monitor circuit further comprises a path comprising the third

MOS transistor and the fourth MOS transistor and simulating the critical path, and outputting the delay signal by simulating the delay time.

8. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages to a first circuit comprised of a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type, comprising:

outputting a delay signal from a delay monitor circuit comprising a third MOS transistor of [[a]] the first conductivity type and a fourth MOS transistor of [[a]] the second conductivity type,

comparing the delay signal with a clock signal by a first comparator,

outputting a first control signal and a second control signal from the comparator,

outputting a difference signal from a compensation circuit, the difference signal based on a difference between a threshold voltage of a fifth MOS transistor of a first conductivity type and a sixth MOS transistor of a second conductivity type,

adjusting the second control signal using the difference signal in comparison to the first control signal, and

outputting [[a]] the first well bias voltage controlled by the first control signal to the first and third MOS transistors, and outputting [[a]] the second well bias voltage controlled by the second control signal adjusted by the difference signal to the second and fourth MOS transistors.

9. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages according to claim 8, further comprising:

outputting a first logical threshold voltage from a first CMOS inverter, the first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor,

outputting a first reference voltage and a second reference voltage lower than the first reference voltage from a reference voltage generator,

comparing the first logical threshold voltage with the first and second reference voltages by a second comparator,

outputting a first signal and a second signal from the second comparator to a difference detector, and

outputting the difference signal by detecting a difference of the first signal and the

second signal in the difference detector.

10. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages according to claim 9, further comprising:

outputting the first signal when the first logical threshold voltage is higher than the first reference voltage, and outputting the second signal when the first logical threshold voltage is lower than the second reference voltage.

11. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages according to claim 8, further comprising:

outputting a first logical threshold voltage from a first CMOS inverter, the first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor,

comparing the first logical threshold voltage with a second logical threshold voltage of a second CMOS inverter, and with a third logical threshold voltage of a third CMOS inverter by a second comparator,

outputting a first signal and a second signal from the second comparator to a difference detector, and

outputting the difference signal by detecting a difference of the first signal and the second signal in the difference detector.

12. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages according to claim 11, further comprising:

outputting the first signal when the first logical threshold voltage is higher than the second threshold voltage, and outputting the second signal when the first logical threshold voltage is lower than the third logical threshold voltage.

13. (Currently Amended) An output method for outputting [[a]] first and second well bias voltages according to claim 8, further comprising:

adjusting the second control signal using the difference signal in comparison to the first control signal by using a table lookup method.

14. (Currently Amended) An output method for outputting [[a]] first and second well bias

voltages according to claim 8, further comprising:

simulating a delay time in a critical path comprising the first MOS transistor and the second MOS transistor by a path comprising the third MOS transistor and the fourth MOS transistor, and

outputting the delay signal from the delay monitor [[signal]] circuit by simulating the delay time.

IN THE DRAWINGS:

Please enter the attached corrected drawings Figs. 12-13, wherein a circuit connecting point is being shifted from vban to vbap in Fig. 12 and a reference number "135" is being changed into "35" in Fig. 13, to replace Figs. 12-13 as originally filed. A Letter to Draftsperson is also submitted herewith.

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated June 29, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-14 are under consideration in this application. Claims 1-6 and 8-14 are being amended as requested by the Examiner. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Objections and Rejection

The drawings were objected to for various informalities, including various errors in the reference numerals and reference terms used in the drawings. The Title of the Invention was objected for being non-descriptive of the claimed invention, but has suggested an alternative wording that he would find acceptable. The Abstract of the Disclosure and the specification were objected to for other informalities. Claims 2, 3, 6 and 8-14 were objected to for various informalities in the wording of the claims, and claims 2-5 and 8-14 were rejected under 35 USC §112, second paragraph, for being indefinite. As indicated, the claims, the specification and drawings have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality objection and rejection is in order, and is therefore respectfully solicited.

Double Patenting Rejection

Claims 1-14 were rejected under judicially created doctrine of obviousness-type double patenting as being unpatentable over at least claim 1 of U.S. Patent No. 6,653,890, which is the parent application of this currently pending application. The Examiner contended that although the claims are not identical, however, they are not patentably distinct. A terminal disclaimer is being submitted according to the Examiner's suggestion. Accordingly, the withdrawal of the outstanding double patenting rejection is in order, and is respectfully solicited.

Allowed Subject Matters

Claims 1-14 would be allowed if all formal objections, and the formal and double-patenting rejections could be overcome. As the claims are being amended as required by the Examiner, they are in condition for allowance.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200
September 29, 2004

SPF/JCM/JT

PART B - ISSUE FEE (S) TRANSMITTAL

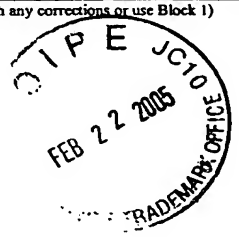
Complete and mail this form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate FEE ADDRESS for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

REED SMITH LLP
SUITE 1400
3110 FAIRVIEW PARK DRIVE
FALLS CHURCH, VA 22042



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Certificate of Mailing

I hereby certify that this Issue Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelop addressed to the Box Issue Fee address on the date indicated below..

(Depositor's name)
(Signature)
(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,477	09/29/2003	Goichi Ono	NITT.0156	1514

TITLE OF INVENTION: WELL BIAS VOLTAGE CONTROL CIRCUIT AND METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1370	$300	$1670	01/21/2005

EXAMINER	ART UNIT	CLASS - SUBCLASS
ENGLUND, TERRY LEE	2816	327-537000

1. Change of correspondence address or indication of ☐Fee Address" (37 CFR §1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (have as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed

1. Reed Smith LLP
2. Stanley P. Fisher, Esq.
3. Juan Carlos A. Marquez, Esq.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **RENESAS TECHNOLOGY CORPORATION**

(B) RESIDENCE: (CITY and STATE OR COUNTRY): **Tokyo, Japan**

Please check the appropriate assignee category indicated below (will not be printed on the patent) ☐ individual ☒ Corporation or private group entity ☐ government

4a. The following fees are enclosed:

☒ Issue fee

☒ Publication Fee

☒ Advance Order - # of Copies: 3

4b. Payment of Fee(s):

☒ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 08-1480 (enclose an extra copy of this form).

The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee and Publication Fee (if any) to the application identified above.

(Authorized Signature) (Date) November 12, 2004

Stanley P. Fisher Reg. No. 24,344 Juan C.A. Marquez Reg. No. 34,072

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered patent attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office

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